

#18/F/D  
6/19/2  
Juslin

PATENT APPLICATION  
ATTORNEY DOCKET NO. Q60098

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Yoko HORIGUCHI

Appln. No.: 09/615,705

Confirmation No.: 4487

Filed: July 13, 2000

For: SEMICONDUCTOR INTEGRATED CIRCUIT



Group Art Unit: 2811

Examiner: O. Nadav

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JUN 14 2002  
TECHNOLOGY CENTER 2800

**SUBMISSION OF CORRECTED FORMAL DRAWINGS**

Commissioner for Patents  
Washington, D.C. 20231

Sir:

Submitted herewith please find nine (9) sheets of corrected Formal Drawings. The Examiner is respectfully requested to acknowledge receipt of these corrected Formal Drawings.

The submitted drawings incorporate the proposed drawing changes approved in Paper Nos. 9 and 12.

Respectfully submitted,

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Date: June 13, 2002



Fig. 1

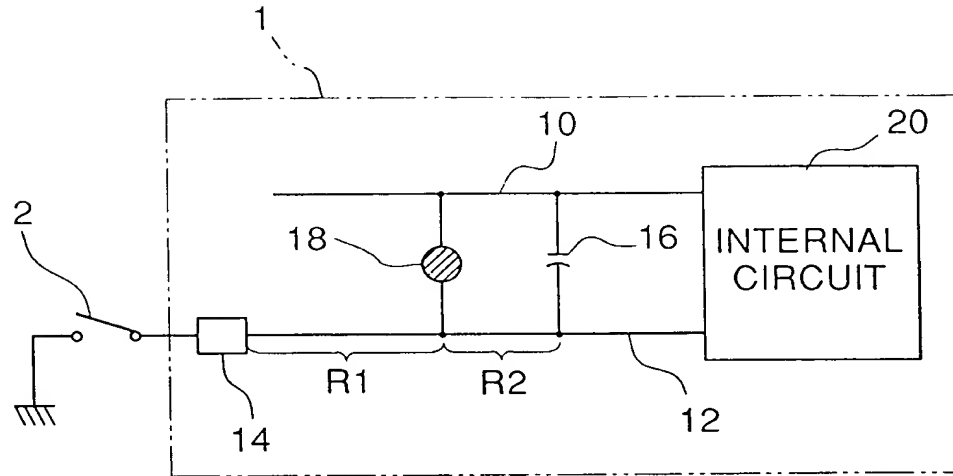


Fig. 2

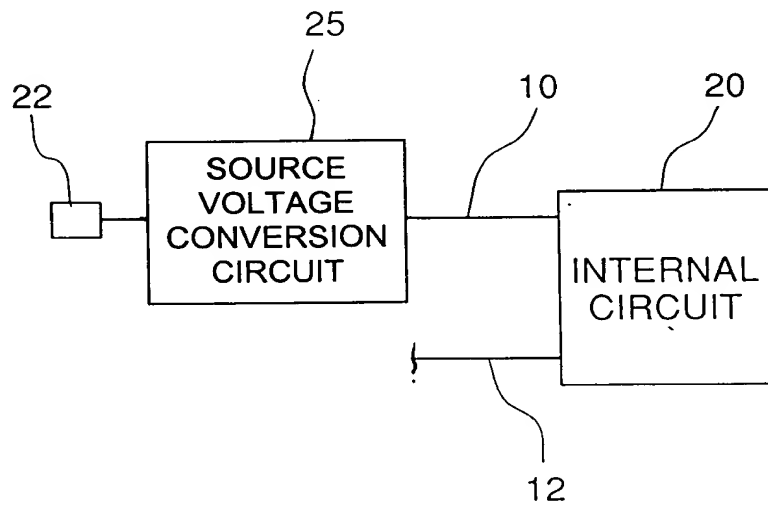


Fig. 3

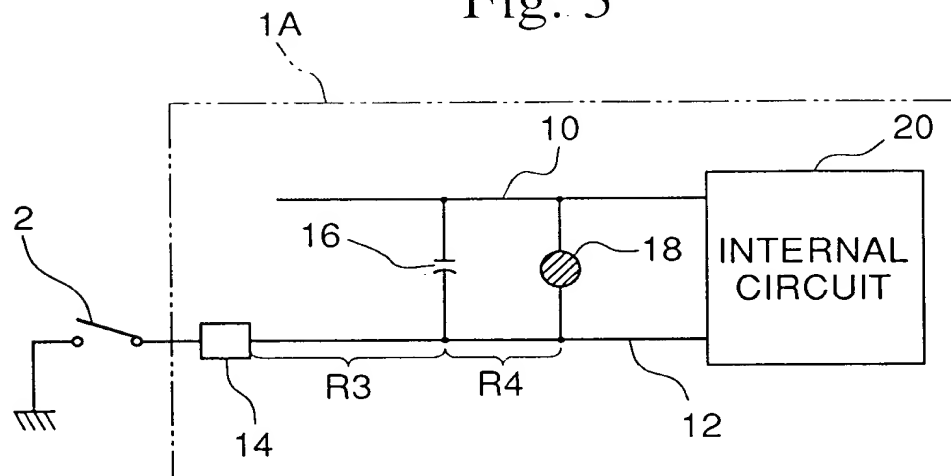


Fig. 4

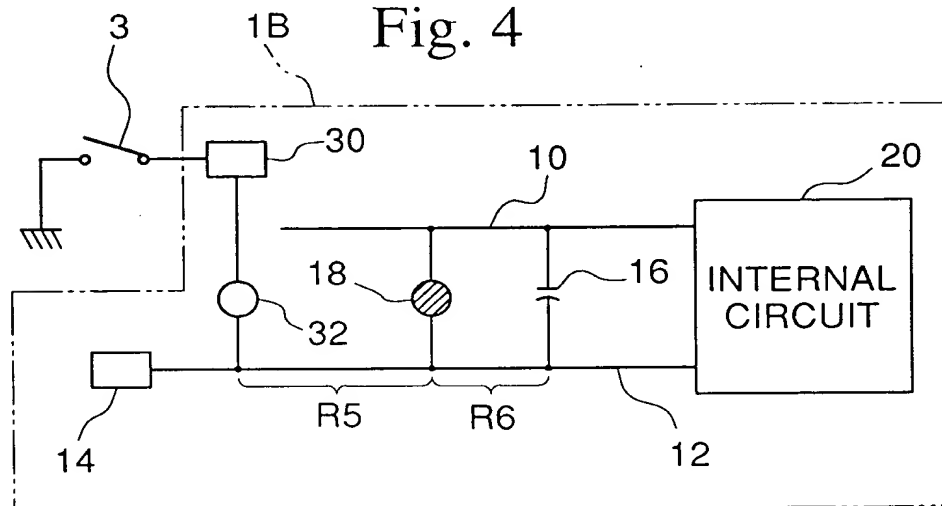


Fig. 5

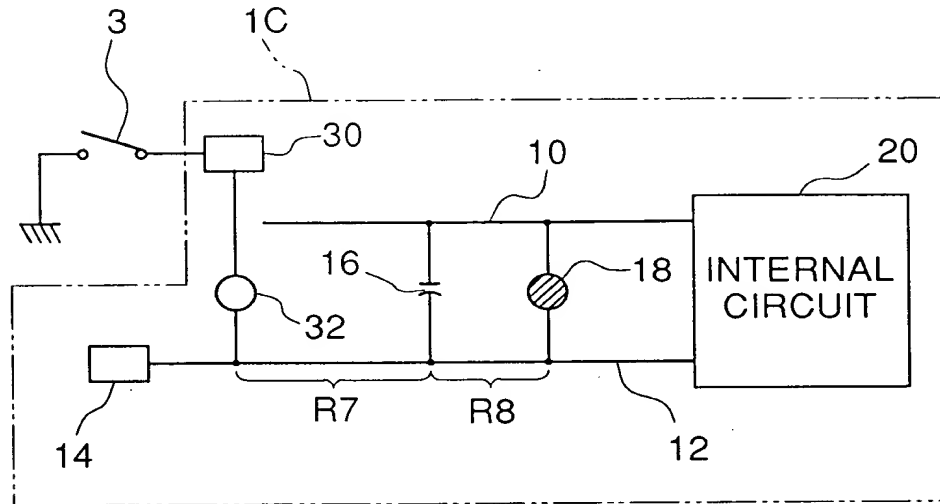


Fig. 6

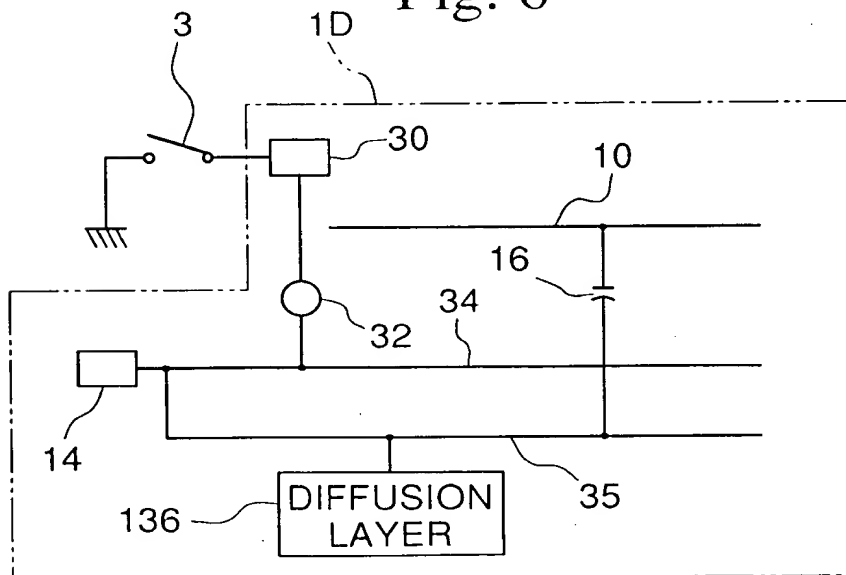


Fig. 7

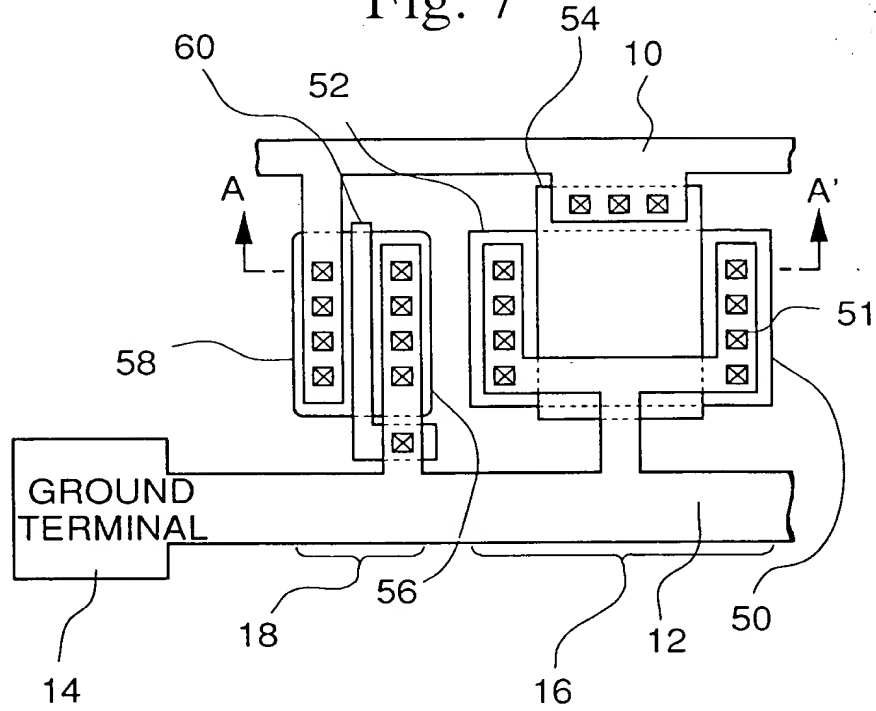


Fig. 8

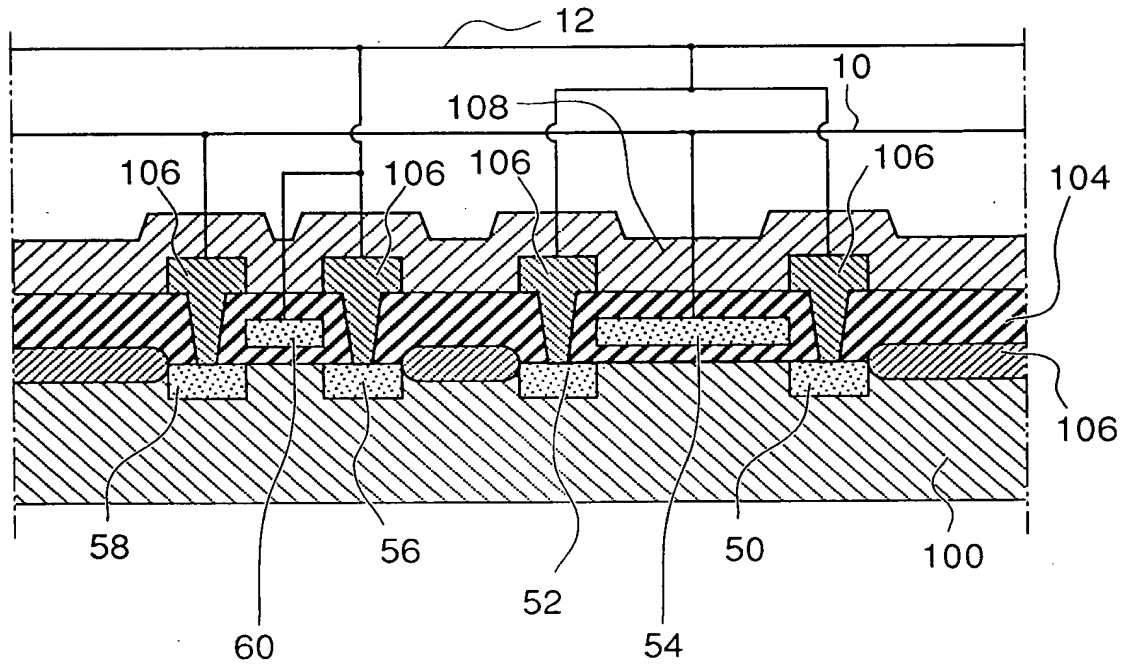


Fig. 9

Diagram illustrating a multi-channel signal processing circuit, labeled Fig. 9. The circuit includes an INPUT/OUTPUT TERMINAL (30) connected to a series of input channels (18, 50, 51). Each channel contains a series of input elements (52, 54) and output elements (51). The output elements are connected to a common output line (12) which leads to a GROUND TERMINAL (14). The circuit is divided into sections (16, 18, 50) and includes a central control or timing section (70). Arrows B and B' indicate signal flow directions.

Fig. 11

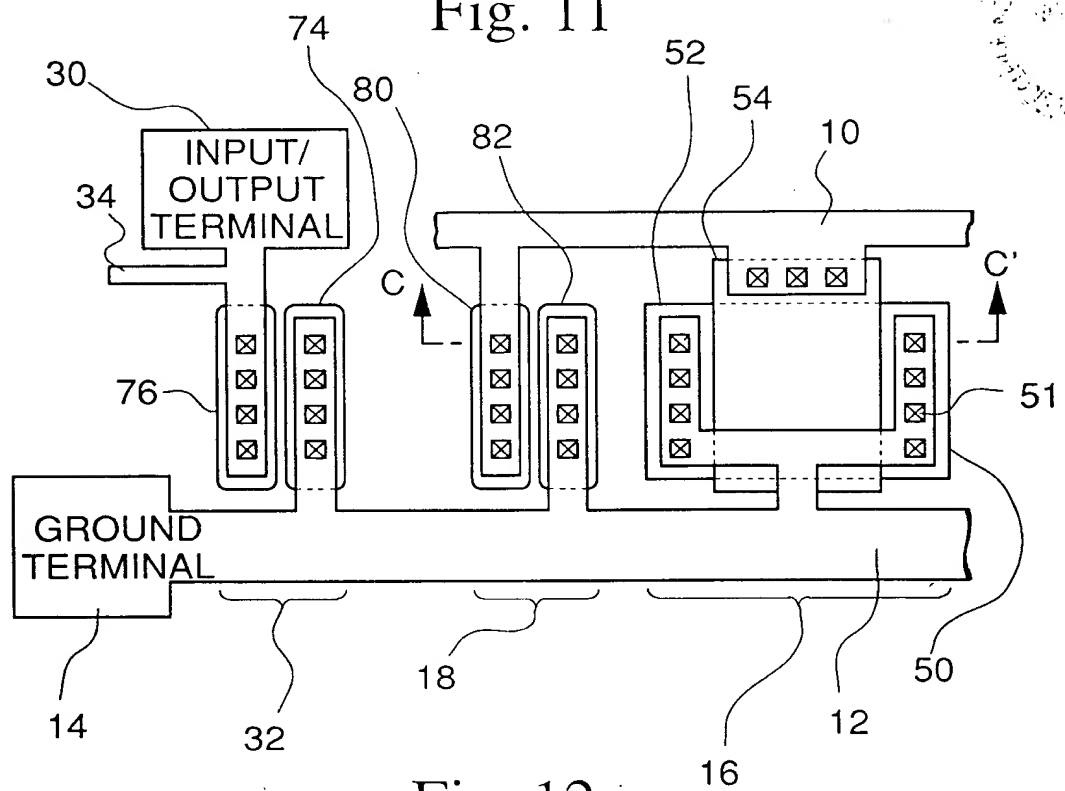
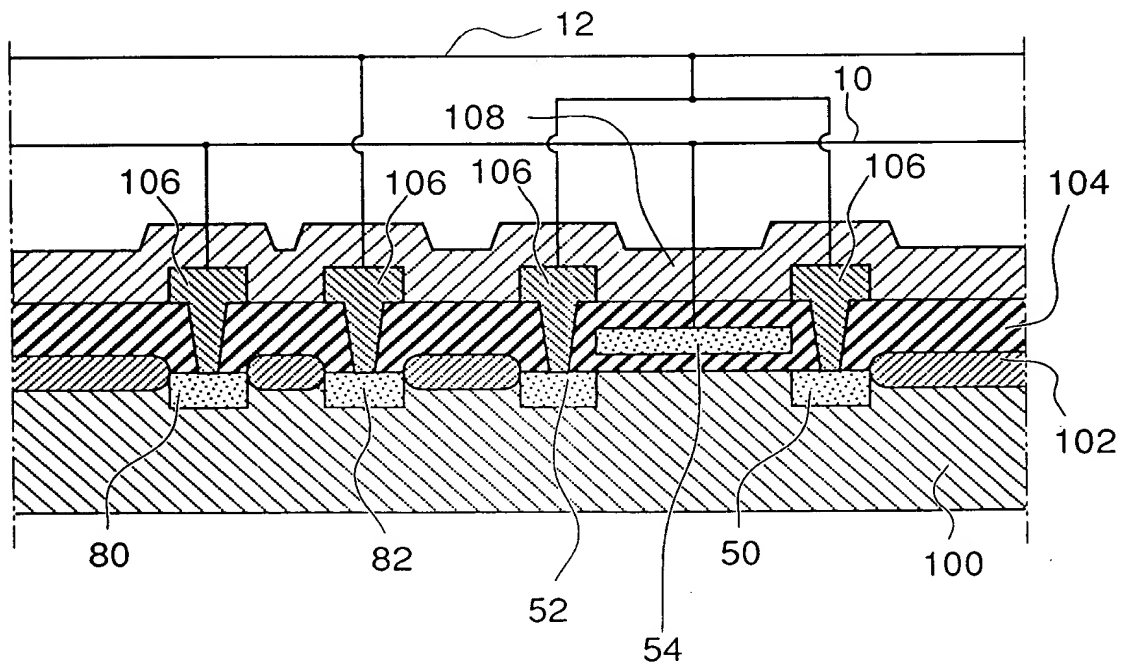


Fig. 12



[illegible]



Fig. 15 PRIOR ART

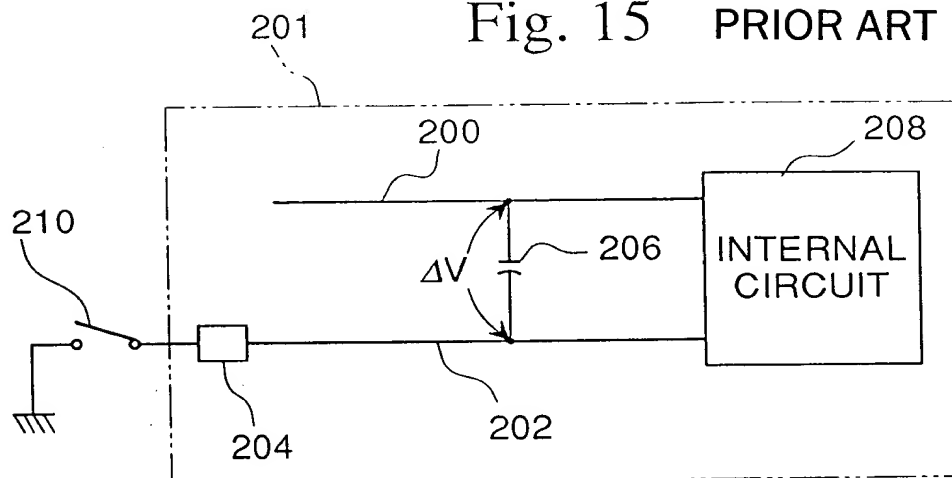


Fig. 16  
PRIOR ART

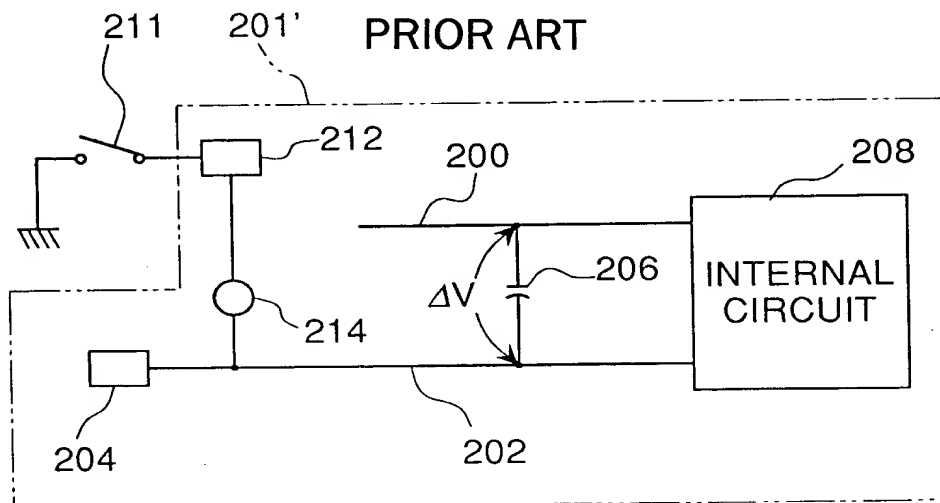


Fig. 17  
PRIOR ART

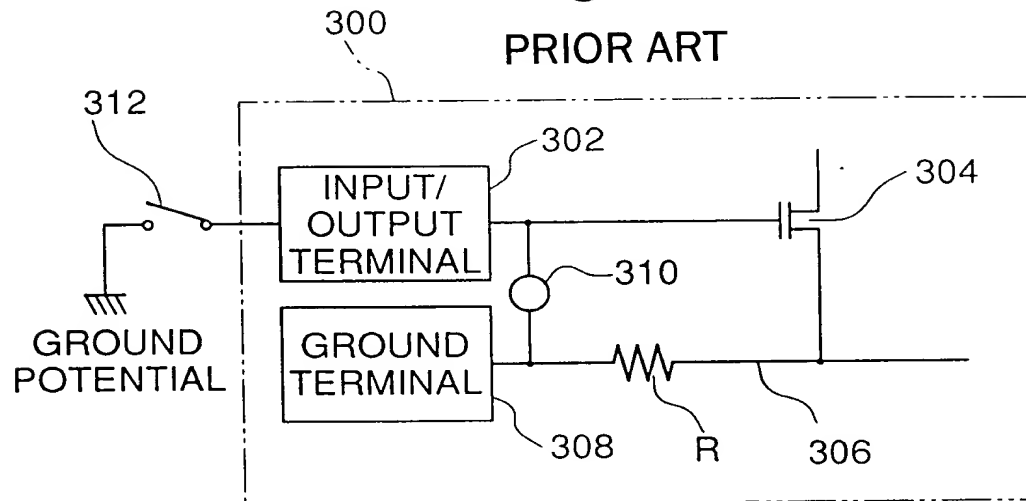


Fig. 18

